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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/751,215	12/29/2000	Andrew Yeoh	042390.P10048	8879

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EXAMINER	
VU, HUNG K	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 10/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/751,215	YEOH, ANDREW	
	Examiner	Art Unit	
	Hung Vu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *5 and 6* is/are allowed.

6)☒ Claim(s) *1,3 and 4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *08/10/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Request for Continued Examination

1 A request for continued examination (RCE) under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant ' submission filed on 08/10/04 has been entered. An action on the RCE follows.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3 and 4 rejected under 35 U.S.C. 103(a) as being unpatentable over Edelstein et al. (PN 6,181,012, of record).

Edelstein et al. discloses, as shown in Figures 2 – 4D, a method for forming hardened interconnects comprising:

depositing a metal layer (76,78,86) comprising copper and an additional metal species comprising beryllium over a semiconductor wafer surface;

after depositing the metal layer comprising copper and an additional metal species comprising beryllium, performing chemical-mechanical polishing of the deposited metal layer comprising copper and an additional metal species comprising beryllium. Note that it is inherent that the additional metal species hardens the deposited metal layer to reduce the rate of the polishing [Col. 6, lines 24-50 and Col. 7, lines 21-33].

Edelstein et al. does not disclose the copper and an additional metal species are co-deposited. However, Edelstein et al. discloses, as shown in Figure 1 and Col. 2, lines 45-65, methods of forming interconnects wherein a copper and an additional metal species are co-deposited. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to co-deposit the copper and an additional metal species, such as taught by Figure 1 of Edelstein et al. since co-deposition process is commonly used to form the interconnects.

With regard to claim 3, Edelstein et al. discloses depositing the metal layer comprising copper and the additional metal species comprising beryllium comprises depositing the metal layer and the additional metal species over an at least one opening in an insulating layer formed over the semiconductor wafer surface.

With regard to claim 4, it is inherent that the additional metal species comprising beryllium forms a solid solution in the deposited metal layer.

3. Claims 1, 3 and 4 rejected under 35 U.S.C. 103(a) as being unpatentable Shimomura (PN 6,352,920, of record) over Edelstein et al. (PN 6,181,012, of record).

Shimomura discloses, as shown in Figure 3(c), a method for forming hardened interconnects comprising:

depositing a metal layer (17) comprising copper and an additional metal species comprising beryllium over a semiconductor wafer surface;

after depositing the metal layer comprising copper and an additional metal species comprising beryllium, performing chemical-mechanical polishing of the deposited metal layer comprising copper and an additional metal species comprising beryllium. Note that it is inherent that the additional metal species hardens the deposited metal layer to reduce the rate of the polishing [Col. 5, lines 7-47].

Shimomura does not disclose the copper and an additional metal species are co-deposited. However, Edelstein et al. discloses methods of forming interconnects wherein a copper and an additional metal species are co-deposited. Note Figure 1 and Col. 2, lines 45-65. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the interconnects of Shimomura by co-depositing the copper and an additional metal species, such as taught by Figure 1 of Edelstein et al. since co-deposition process is commonly used to form the interconnects.

With regard to claim 3, Edelstein et al. discloses depositing the metal layer comprising copper and the additional metal species comprising beryllium comprises depositing the metal layer and the additional metal species over an at least one opening in an insulating layer formed over the semiconductor wafer surface.

With regard to claim 4, it is inherent that the additional metal species comprising beryllium forms a solid solution in the deposited metal layer.

4. Claims 1, 3 and 4 rejected under 35 U.S.C. 103(a) as being unpatentable over Pavate et al. (PN 6,432,819, of record) in view of Edelstein et al. (PN 6,181,012, of record).

Pavate et al. discloses, as shown in Figure 2, a method for forming hardened interconnects comprising:

depositing a metal layer (210) comprising copper and an additional metal species comprising beryllium over a semiconductor wafer surface;

after depositing the metal layer comprising copper and an additional metal species comprising beryllium, performing chemical-mechanical polishing of the deposited metal layer comprising copper and an additional metal species comprising beryllium. Note that it is inherent that the additional metal species hardens the deposited metal layer to reduce the rate of the polishing [Col. 6, lines 8-20, lines 35-38 and lines 55-65].

Pavate et al. does not disclose the copper and an additional metal species are co-deposited. However, Edelstein et al. discloses methods of forming interconnects wherein a copper and an additional metal species are co-deposited. Note Figure 1 and Col. 2, lines 45-65. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the interconnects of Pavate et al. by co-depositing the copper and an additional metal species, such as taught by Figure 1 of Edelstein et al. since co-deposition process is commonly used to form the interconnects.

With regard to claim 3, Pavate et al. and Edelstein et al. discloses depositing the metal layer comprising copper and the additional metal species comprising beryllium comprises depositing the metal layer and the additional metal species over an at least one opening in an insulating layer formed over the semiconductor wafer surface.

With regard to claim 4, it is inherent that the additional metal species comprising beryllium forms a solid solution in the deposited metal layer.

Allowable Subject Matter

5. Claims 5 and 6 are allowed.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hung K. Vu whose telephone number is (571) 272-1666. The examiner can normally be reached on Mon-Thurs 6:00-3:30, alternate Friday 7:00-3:30, Eastern Time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (571) 272-1732. The Central Fax Number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Vu

October 19, 2004

Hung Vu

Patent Examiner